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Question Paper Code: 42443

B.E./B.Tech. DEGREE EXAMINATION, APRIL/MAY 2018

Third Semester

Electronics and Communication Engineering
EC 2205 – ELECTRONIC CIRCUITS – I
(Common to Medical Electronics Engineering)
(Regulations 2008)

Time: Three Hours

Maximum: 100 Marks

Answer ALL questions

PART - A

 $(10\times2=20 \text{ Marks})$

- 1. What is the role of collector resistance RC?
- 2. List out the advantages of voltage divider bias.
- 3. Compare the characteristics of CE, CB and CC amplifiers.
- 4. Define CMRR. How to improve it?
- 5. Draw high frequency equivalent circuit diagram of BJT device.
- 6. Find the unity gain bandwidth of MOSFET whose $g_m = 6$ mA/V, $C_{gs} = 8pF$ and $C_{gd} = 4pF$.
- 7. Define Cross-over distortion. How to overcome it?
- 8. Define Heat sink.
- 9. Draw the circuit diagram of zener voltage regulator.
- 10. Define SMPS.



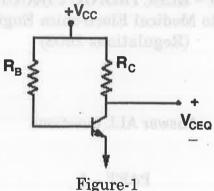
PART - B

(5×16=80 Marks)

11. a) Determine the stability factor due to change in h_{fe} and V_{BE} of voltage divider bias circuit. (16)

(OR)

b) The device parameters for the circuit configuration given in Figure-1 are $h_{\rm fe}=100$ and $V_{\rm BE(on)}=0.7V$. The circuit is to be biased with $V_{\rm CC}=+10V$ and transistor quiescent values should be $I_{\rm CQ}=1$ mA and $V_{\rm CEQ}=5V$. Calculate $I_{\rm CQ}, V_{\rm CEQ}$ for $h_{\rm fe}=50,\,100,\,150$ and 200 and comment on the results. (16)



- 12. a) Determine the voltage gain and current gain of a darlington pair (BJT) amplifier. (16) (OR)
 - b) Determine the voltage gain, input impedance and output impedance of Common-Gate (FET) amplifier. (16)
- 13. a) Determine the upper cut-off frequency of CE amplifier using miller approximation method. (16)

(OR)

b) For the circuit shown in Figure-2, the NFET transistor parameters are : $g_{m} = 2mA/V, I_{DQ} = 4mA \text{ and } V_{A} = 100V, Cgs = 1pF \text{ and } Cgd = 0.4 pF. \text{ The amplifier has } R_{G} = 100 \text{ k}\Omega, R_{D} = R_{L} = 15 \text{ k}\Omega. \text{ Calculate the mid-band gain, upper cut-off frequency. Also find the values of } C_{G}, C_{D} \text{ and } C_{S} \text{ by assuming lower cutoff frequency of } 100 \text{ Hz and that the nearest break frequency be at least a decade lower.}$

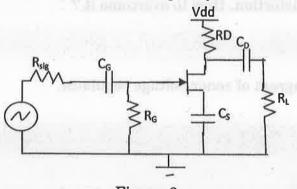


Figure-2



14. a) Determine the maximum power dissipation in a transistor (with and without heat sink). Consider the power device for which the thermal resistance parameters are:

 $\theta_{\text{dev-case}} = 1.75^{\circ}\text{C/W}, \ \theta_{\text{case-sink}} = 1.0^{\circ}\text{C/W}, \ \theta_{\text{sink-amb}} = 5^{\circ}\text{C/W} \ \text{and} \ \theta_{\text{case-amb}} = 50^{\circ}\text{C/W}.$ The ambient temperature is $T_{\text{amb}} = 30^{\circ}\text{C}$ and the maximum junction or device temperature $T_{\text{jma}}x = T_{\text{dev}} = 150^{\circ}\text{C}$. Comment on the results. (16)

- b) Determine the maximum conversion efficiency of Class-A power amplifier. (16)
- 15. a) Explain the Half-wave rectifier in terms of average value of output voltage and current, Ripple factor and Rectification efficiency. (16)

 (OR)
 - b) Explain how the output voltage is controlled by zener voltage regulator during varying input voltage and variable load resistance. (16)

- 14. a) Determine the maximum power dowingston in a frameion (with and without that coninc the power downs for which the theorem security of the statement of th
- B ___ = 1.75°C/W, B ____ = 1.0°C/W, u_{constant} = 5°C/W and 0 ____ = 6°C/W.

 The imbient temperature in T ___ = 30°C and the meatures provides or device temperature T __ = T __ = 150°C. Comment on the results.

 (18)

(OB)

- b) Determine the reinfurna conversion efficiency of Chats-A power supplifies. (18)
- 15, a) Explain the Half-wave resulter in terms of average value of output voltage and current. Ripple Institute and Restification efficiency.

(STO)

b) Explain how the output voltage is controlled by sener voltage regulator during varying input voltage and variable load resistance.